

ABSTRACT

A non-volatile memory cell structure that is capable of holding two data bits. The structure includes a trench in a substrate with two sides of the trench being lined with a trapping material. The trench is filled with an oxide dielectric material and a control gate is formed over the oxide-filled trench. Source/drain regions are adjacent the trench sides with the trapping material. An energy barrier between the drain and source regions has two local high points that correspond to the trench corners. To read the device, sufficient gate voltage is applied to invert the channel and a sufficient drain voltage is applied to pull down the drain-side barrier. If charges of opposite polarity are trapped in the source-side trench corner, the source barrier will be significantly lowered so that current flows between source and drain under read conditions.